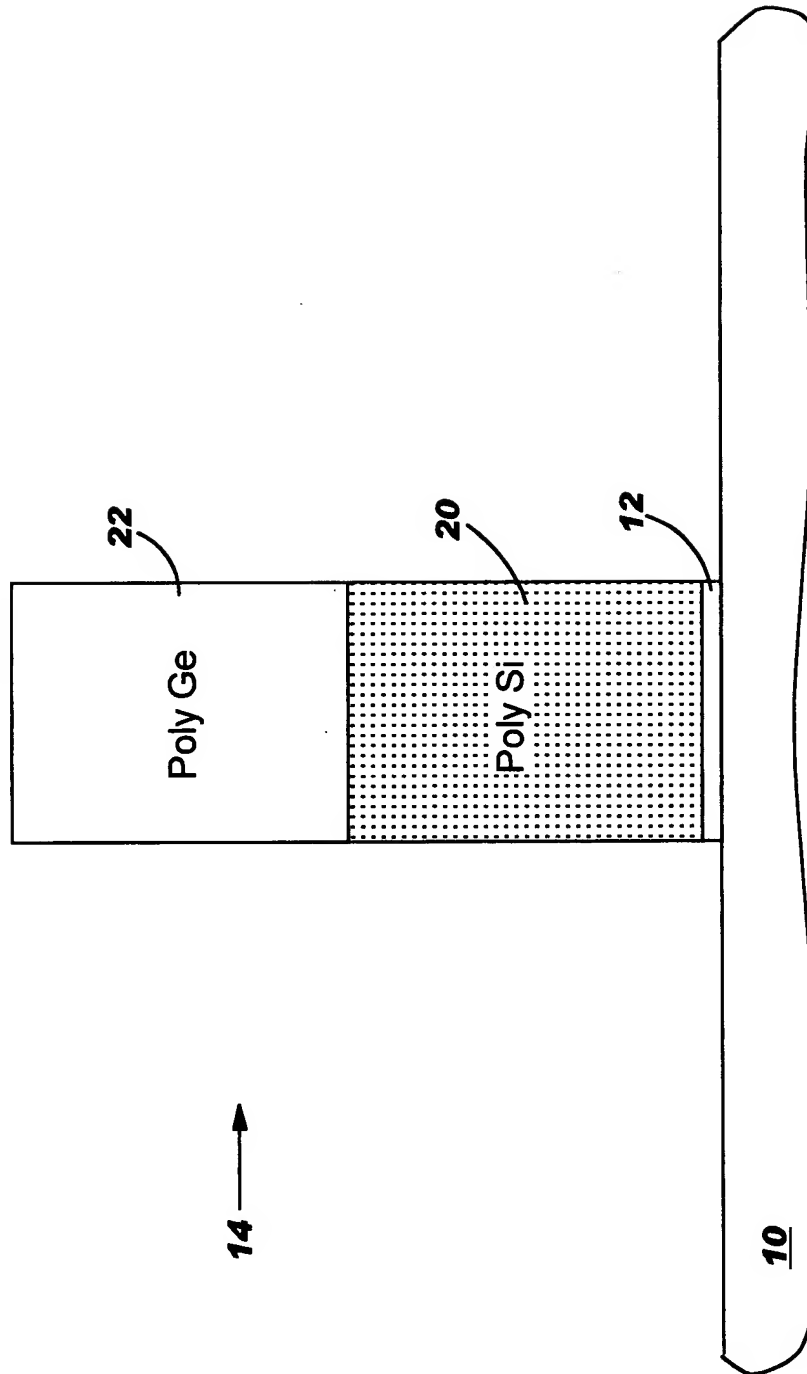




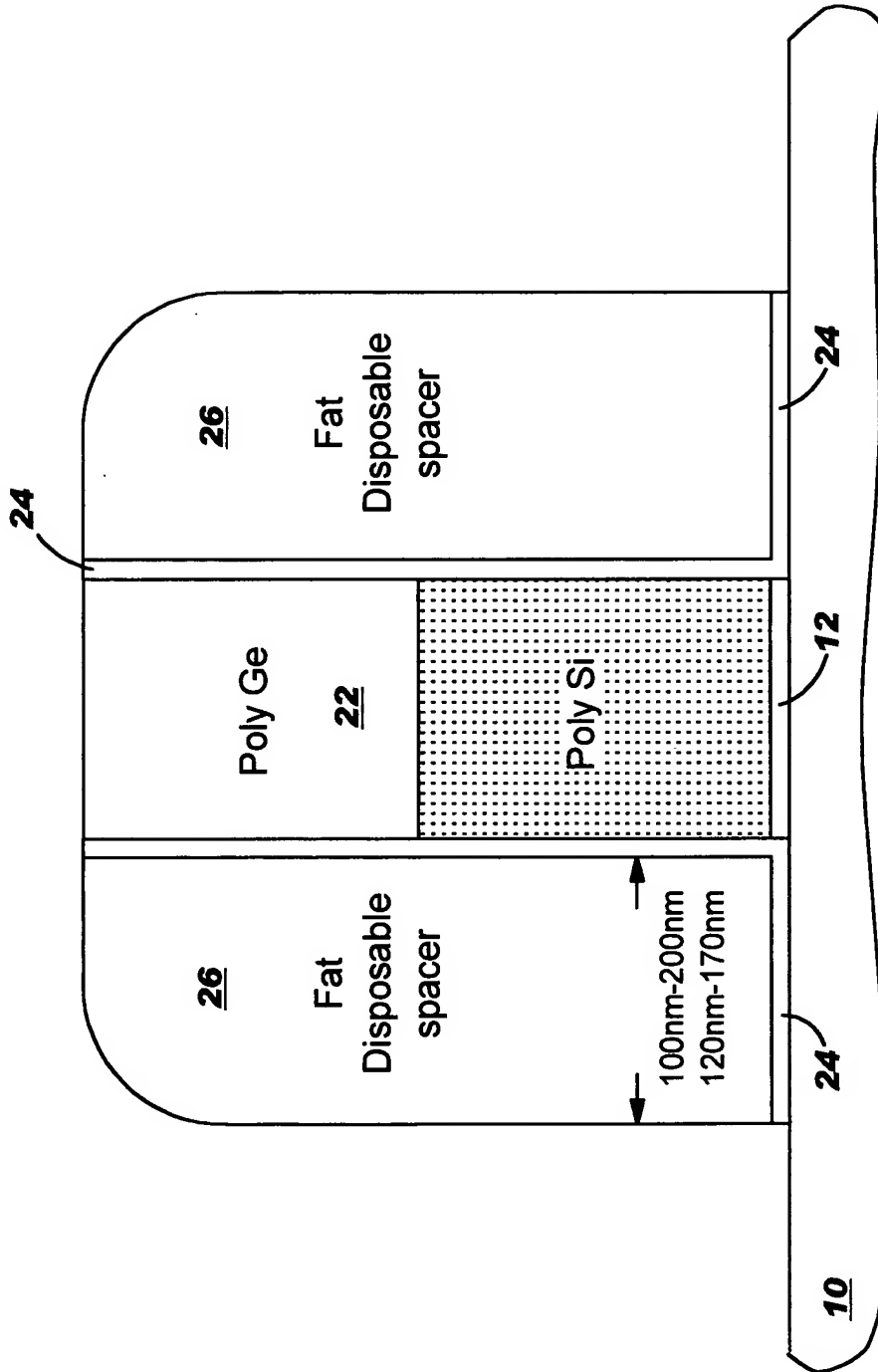
FIG. 1



- STI, N and P Well,
- gate dielectric formation (plasma nitrided thermal oxidation or deposited oxynitride or nitride)
- Intrinsic polySi (~150nm) and intrinsic polyGe (~150nm) deposition
- Poly Si and PolyGe stack etch

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FIG. 2



- Fat Spacer formation
- Oxide/nitride liner deposition
 - Conformal CVD or plasma CVD SiO₂ deposition
 - RIE directional etching of SiO₂

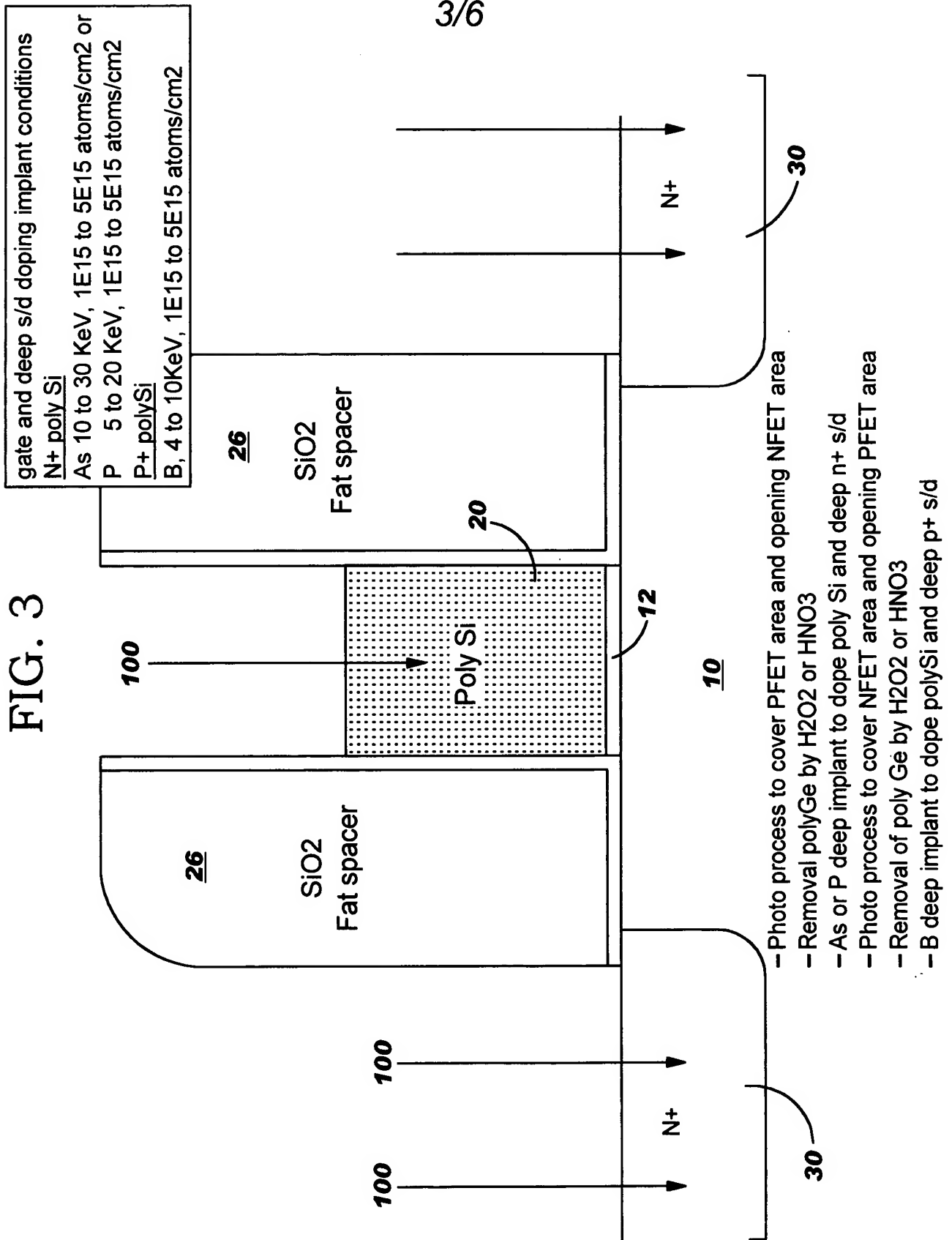
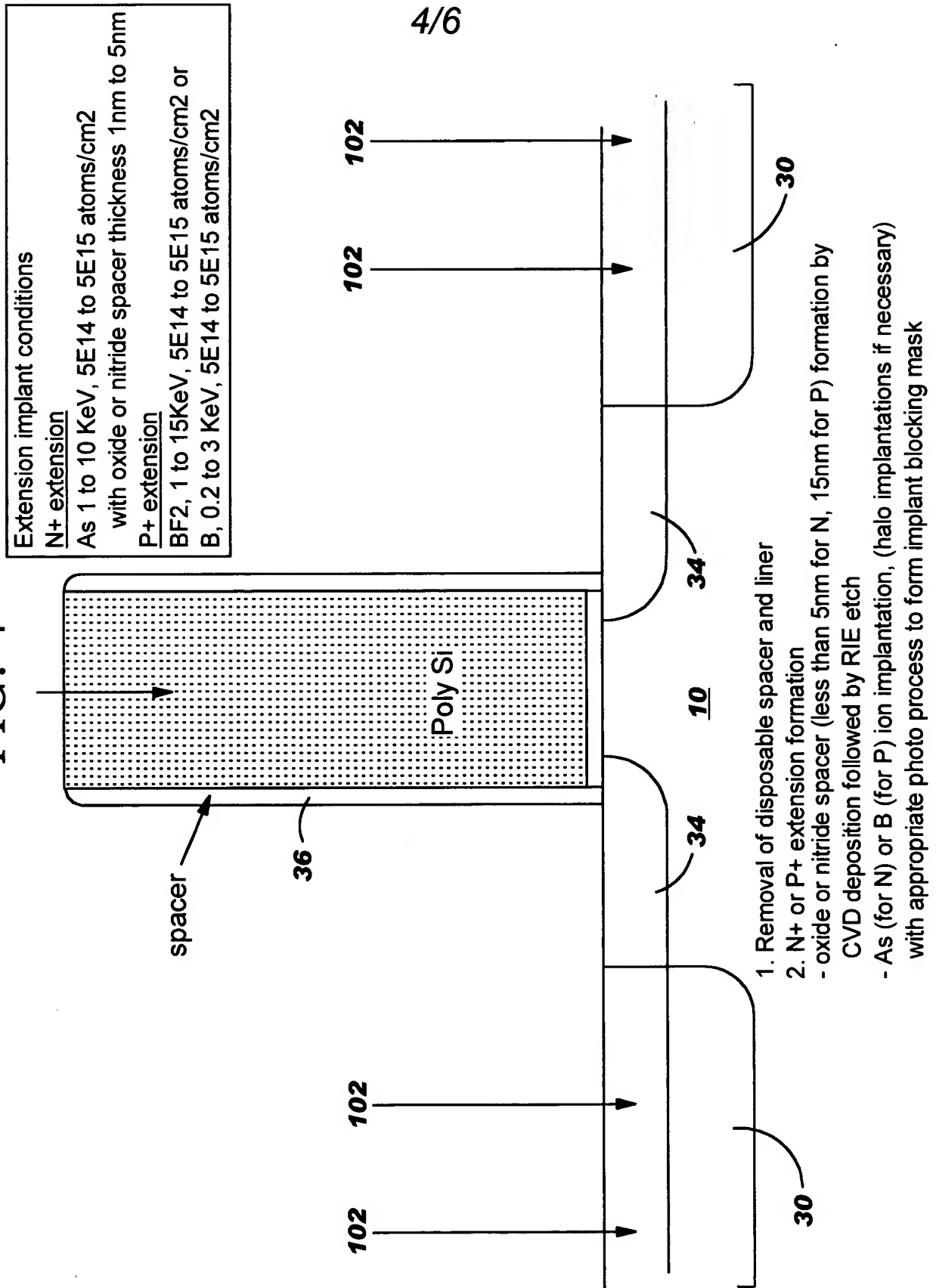
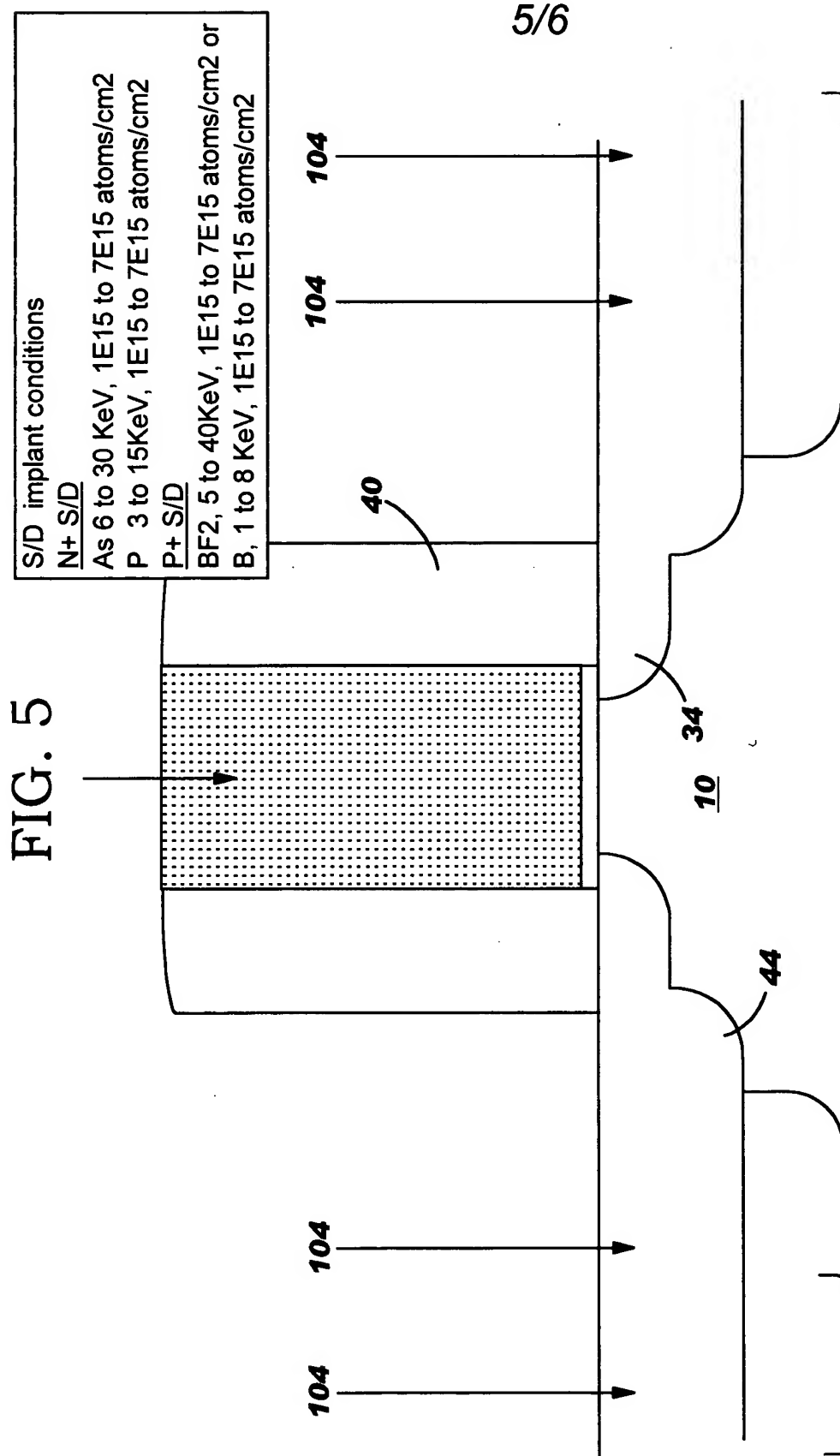


FIG. 4





N+ or P+ S/D diffusion formation

- oxide (or nitride+oxide) spacer (50nm - 100nm) formation by

CVD deposition followed by RIE etch

- As or P (for N+) or B (for P+) ion implantation

with appropriate photo process to form implant blocking mask,

- Strip photo resist after the implants

- Dopant activation anneal at 1000C to 1100C, for 10 sec to 10m sec

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